1. Features

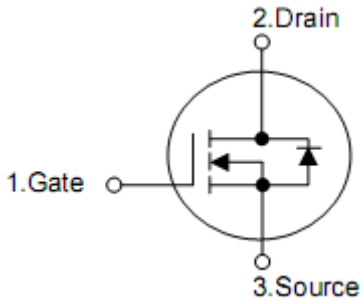
- SGT MOSFET technology
- Proprietary New Planar Technology
- $R_{DS(ON)}$=15mΩ(typ.)@V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

2. Applications

- Synchronous Rectification
- UPS Inverter

3. Pin configuration

TO-252



Pin	Function
1	Gate
2	Drain
3	Source

4. Ordering Information

Part Number	Package	Brand
KCD9310A	TO-252	KIA

5. Absolute maximum ratings

(T_C= 25 ºC , unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-to-Source Voltage [1)]	V_{DSS}	100	V
Gate-to-Source Voltage	V_{GSS}	±20	V
Continuous Drain Current	I_D	42	A
Pulsed Drain Current at V_{GS}=10V	I_{DM}	168	A
Single Pulse Avalanche Energy [3)]	EAS	100	mJ
Power Dissipation	P_D	61	W
Derating Factor above 25°C	P_D	0.49	W/°C
Soldering Temperature Distance of 1.6mm from case for 10 seconds	T_L	300	ºC
Operating and Storage Temperature Range	T_J&T_{STG}	-55 to 150	ºC

Caution: Stresses greater than those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device.

6. Thermal characteristics

Parameter	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.05	ºC/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	75	º C/W

7. Electrical characteristics

(T_J=25°C,unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	100	-	-	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V	-	-	1	uA
		V_{DS}=80V,T_J=125°C	-	-	100	uA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain-to-Source ON Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=14A	-	15	20	mΩ
		V_{GS}=4.5V, I_D=14A	-	21	30	mΩ
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250uA	1.1	2	2.5	V
Forward Transconductance [4]	gfs	V_{DS}=5V,I_D=15A	-	29	-	S
Input Capacitance	C_{iss}	V_{GS}=0V,V_{DS}=50V, f=1.0MHZ	-	935	-	pF
Reverse Transfer Capacitance	C_{rss}		-	6	-	
Output Capacitance	C_{oss}		-	155	-	
Total Gate Charge	Q_g	V_{DD}=50V,I_D=14A, V_{GS}=0~10V	-	20	-	nC
Gate-to-Source Charge	Q_{gs}		-	5	-	
Gate-to-Drain (Miller) Charge	Q_{gd}		-	5	-	
Turn-on Delay Time	$t_{d(ON)}$	V_{DD}=50V, I_D=14A, R_G=2.2Ω,V_{GS}=10V	-	5	-	nS
Rise Time	t_{rise}		-	20	-	
Turn-Off Delay Time	$t_{d(OFF)}$		-	26	-	
Fall Time	t_{fall}		-	8	-	
Continuous Source Current [2]	I_{SD}	Integral PN-diode in MOSFET	-	-	42	A
Pulsed Source Current [2]	I_{SM}		-	-	168	A
Forward Voltage	V_{SD}	I_S=14A, V_{GS}=0V	-	-	1.2	V
Reverse recovery time	t_{rr}	I_F=14A, diF/dt=100A/μs	-	35	-	ns
Reverse recovery charge	Q_{rr}		-	40	-	uC

Note:
1) T_J=+25°C to +150°C
2) Pulse width≤380μs; duty cycle≤2%.
3) EAS:L=1.0mH

8. Test circuits and waveforms

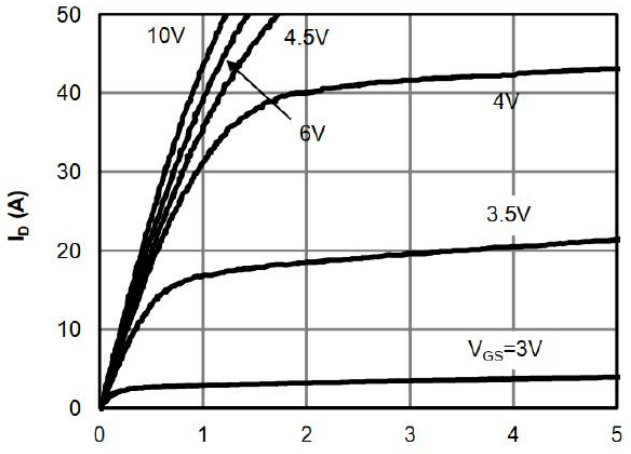


Figure 1: On-Region Characteristics

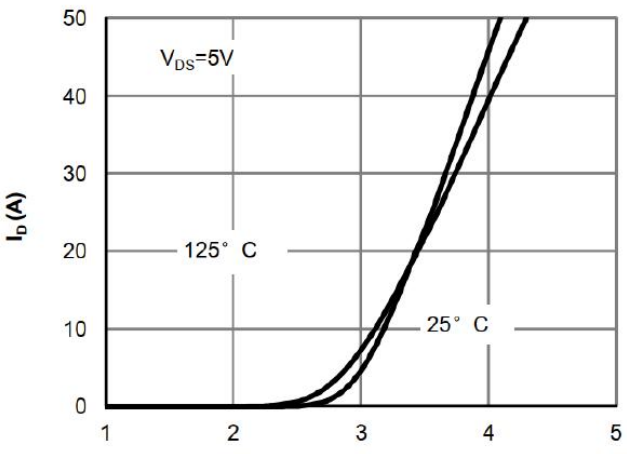


Figure 2: Transfer Characteristics

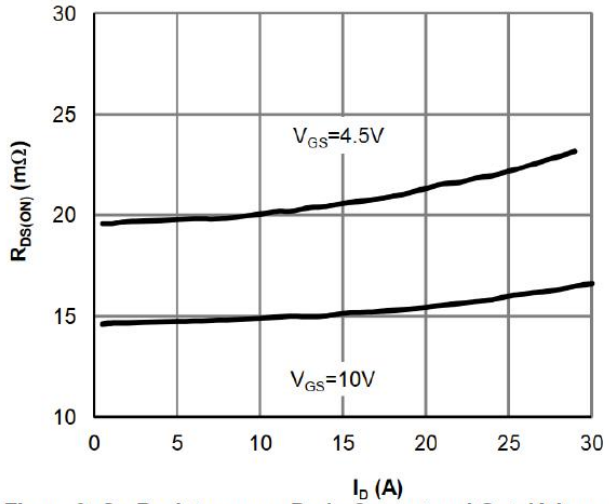


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

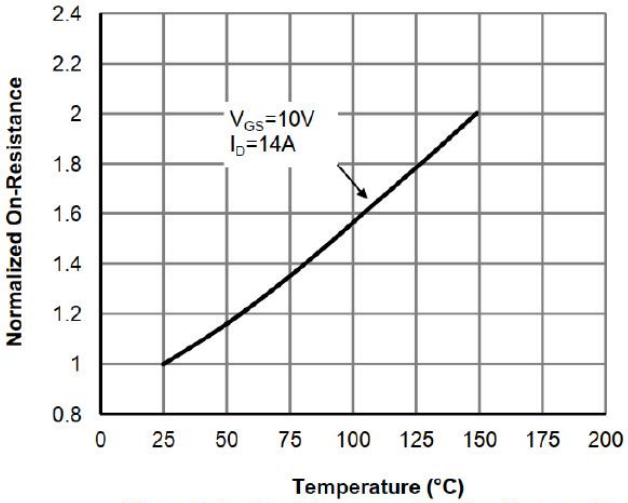


Figure 4: On-Resistance vs. Junction Temperature

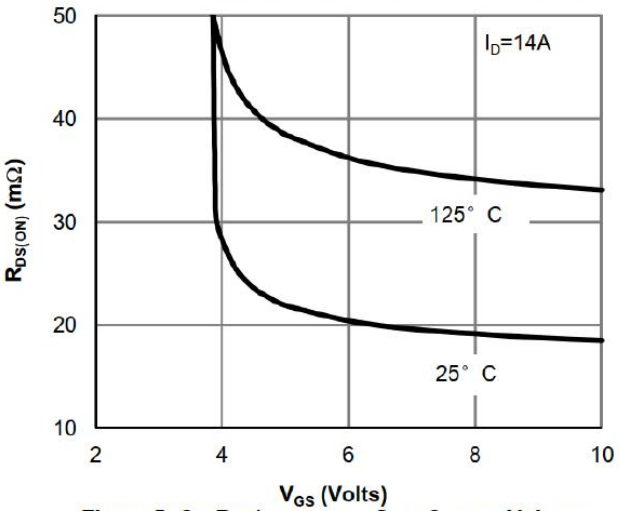


Figure 5: On-Resistance vs. Gate-Source Voltage

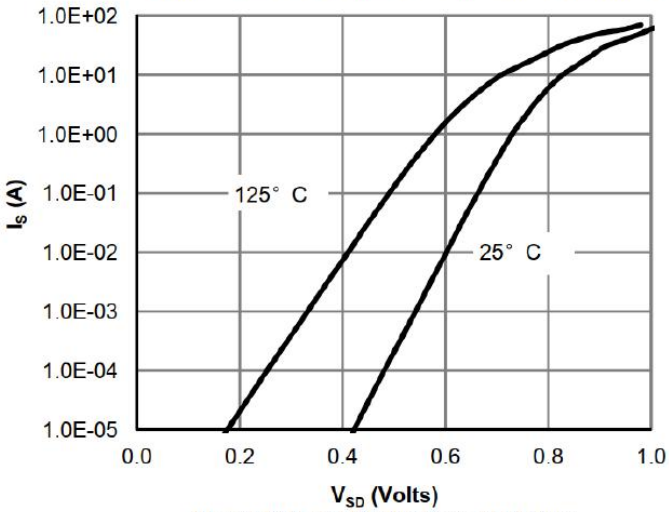


Figure 6: Body-Diode Characteristics

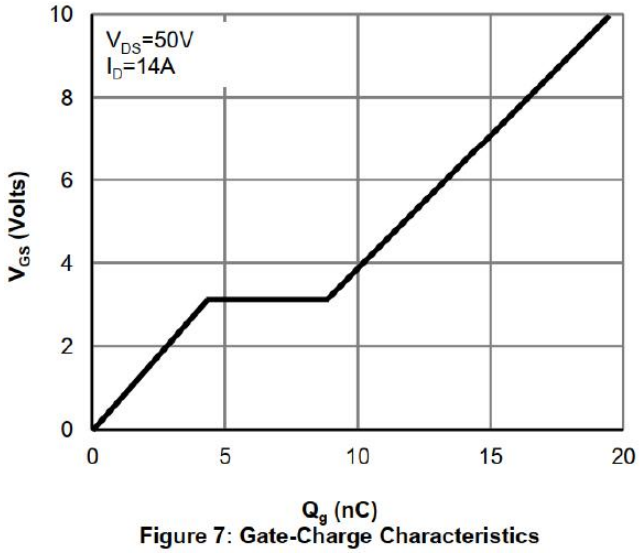


Figure 7: Gate-Charge Characteristics

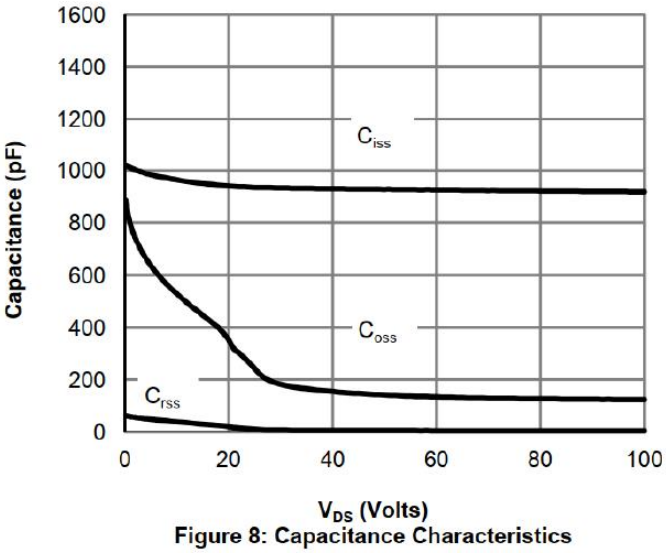


Figure 8: Capacitance Characteristics

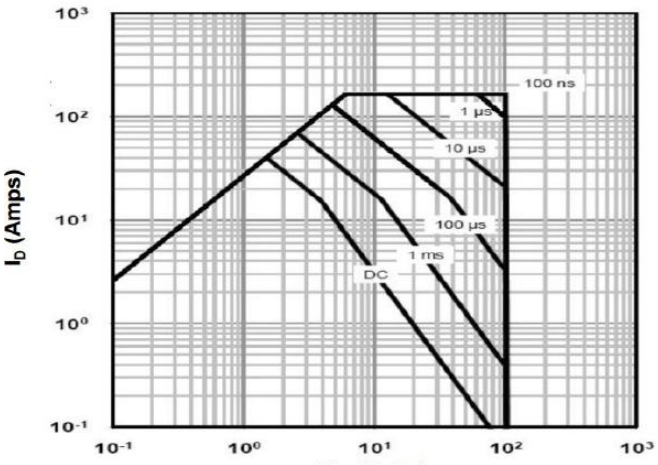


Figure 9: Maximum Forward Biased Safe Operating Area

9. Test Circuits and Waveforms

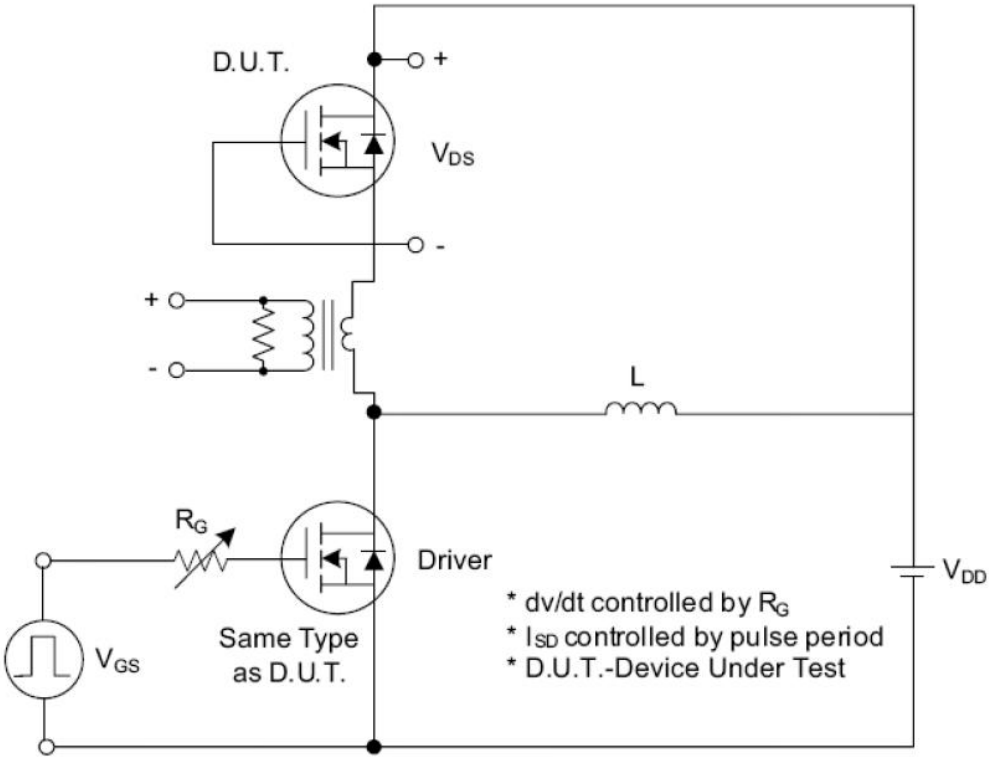


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

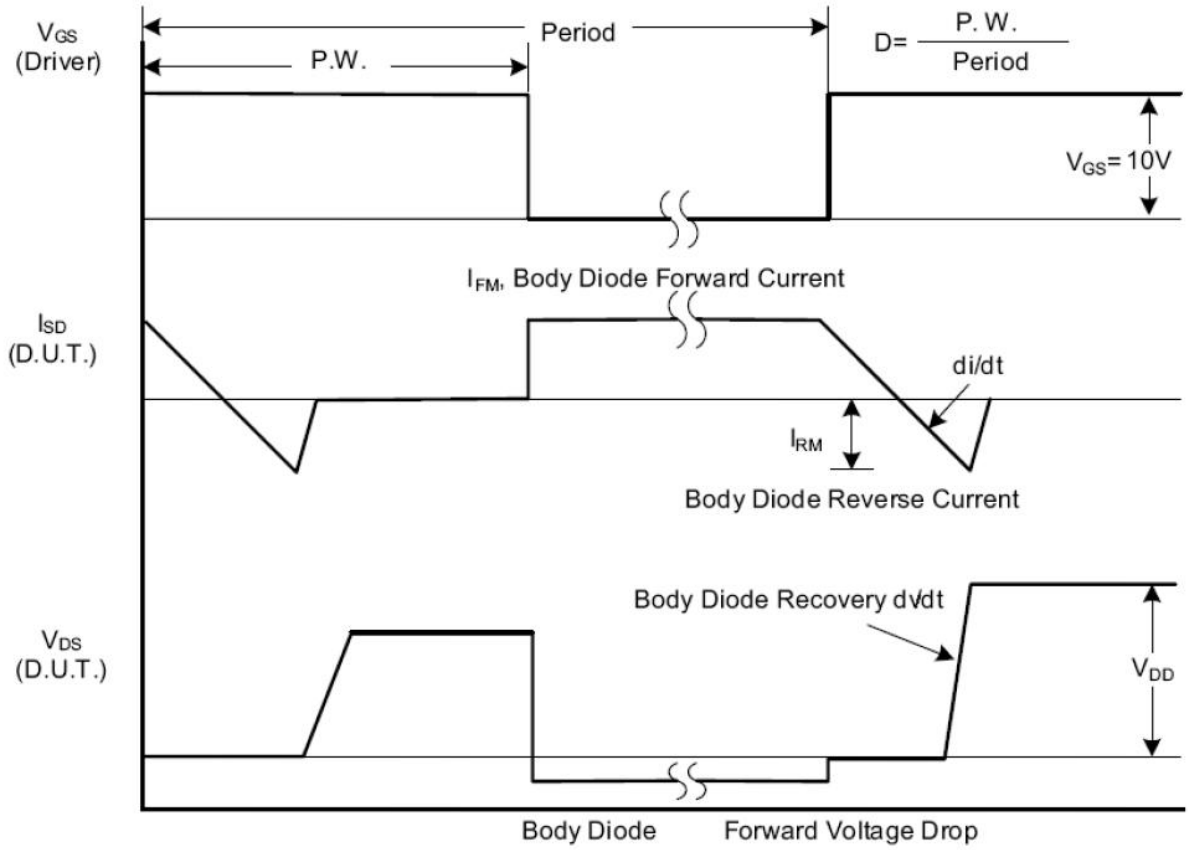


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

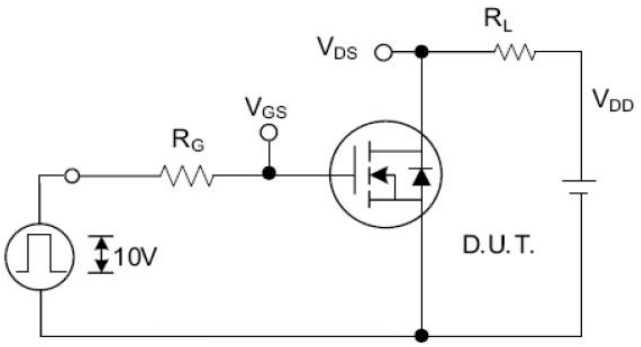


Fig. 2.1 Switching Test Circuit

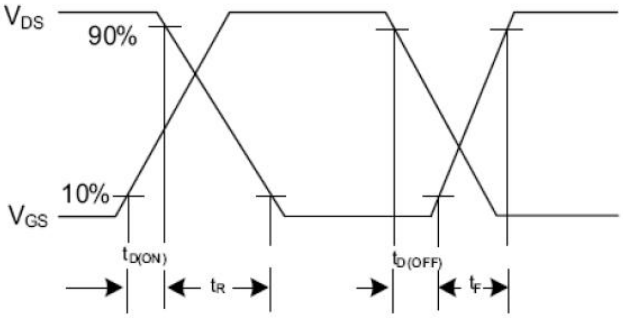


Fig. 2.2 Switching Waveforms

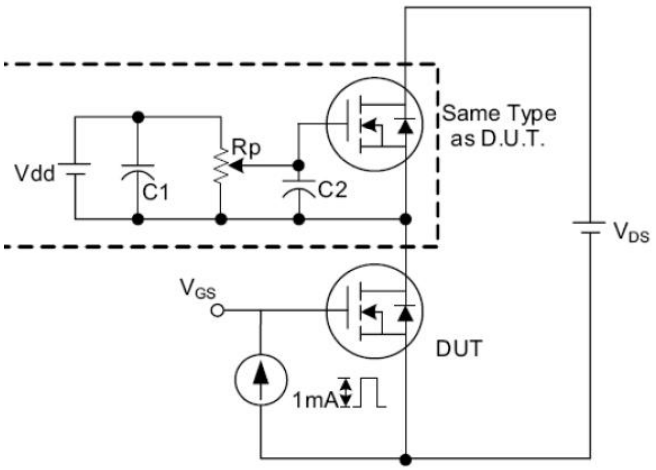


Fig. 3 . 1 Gate Charge Test Circuit

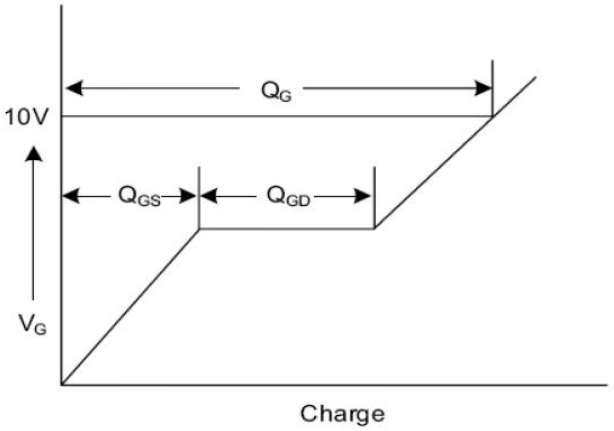


Fig. 3 . 2 Gate Charge Waveform

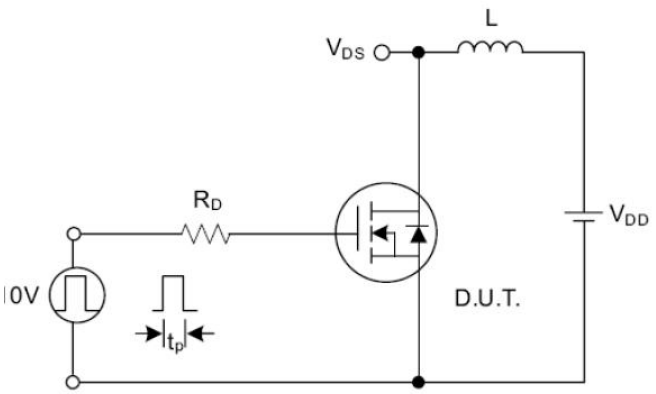


Fig. 4.1 Unclamped Inductive Switching Test Circuit

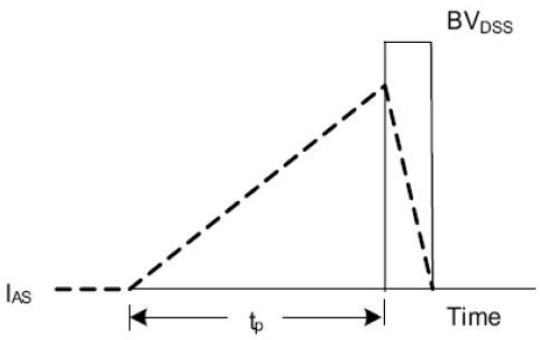


Fig. 4.2 Unclamped Inductive Switching Waveforms