1. Description

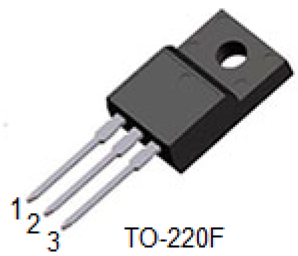
KNX6180B is an N-channel enhancement mode power MOS field effect transistor which is produced using KIA proprietary F-Cell™ high-voltage planar VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

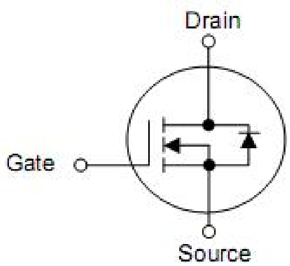
These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.

2. Features

- 10A,800V,$R_{DS(ON)(typ.)}$=0.87Ω @ V_{GS}=10V
- Low Gate Charge
- Low Crss
- Fast switching
- Improved dv/dt capability

3. Pin configuration





Pin	Function
1	Gate
2	Drain
3	Source

4. Ordering Information

Part Number	Package	Brand
KNF6180B	TO-220F	KIA

5. Absolute maximum ratings

T_C=25℃ unless otherwise specified

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DSS}	800	V
Gate-Source Voltage		V_{GSS}	±30	V
Continuous Drain Current	T_C=25°C	I_D	10	A
	T_C=100°C		6.32	A
Pulsed Drain Current at VGS=10V		I_{DM}	40	A
Power Dissipation (T_C=25°C)		P_D	62	W
Derating Factor above 25°C			0.5	W/°C
Single Pulsed Avalanche Energy 1)		EAS	938	mJ
Reverse Diode dv/dt 2)		dv/dt	4.5	V/ns
MOSFET dv/dt Ruggedness 3)		dv/dt	50	V/ns
Operation Junction Temperature Range		T_J	-55 to 150	°C
Storage Temperature Range		T_{STG}	-55 to 150	°C

6. Thermal characteristics

Parameter	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.02	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	°C/W

7. Electrical characteristics

(T_c=25°C,unless otherwise notes)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	800	-	-	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=800V, V_{GS}=0V	-	-	1	uA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250uA	2.0	-	4.0	V
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=5.0A	-	0.87	1.05	mΩ
Gate Resistance	R_g	F=1MHz	-	16	-	Ω
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V F=1.0MHz	-	1625	-	pF
Output Capacitance	C_{oss}		-	152	-	pF
Reverse Transfer Capacitance	C_{rss}		-	6.4	-	pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=400V, R_G=25Ω, I_D=10A 4), 5)	-	28	-	nS
Rise Time	t_r		-	42	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	90	-	nS
Fall Time	t_f		-	75	-	nS
Total Gate Charge	Q_g	V_{DS}=640V,V_{GS}=10V, I_D=10A 4), 5)	-	32	-	nC
Gate-to-Source Charge	Q_{gs}		-	8.5	-	nC
Gate-to-Drain (Miller) Charge	Q_{gd}		-	12	-	nC
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	-	-	10	A
Pulsed Source Current	I_{SM}		-	-	40	A
Diode Forward Voltage	V_{SD}	I_S=10A, V_{GS}=0V	-	-	1.4	V
Reverse Recovery Time	trr	I_S=10A,V_{GS}=0V, dIF/dt=100A/us 4)	-	611	-	ns
Reverse Recovery Charge	Qrr		-	5.6	-	nC

Notes:
1 L=30mH, I_{AS}=7.5A, V_{DD}=100V, R_G=25Ω, starting T_J=25°C;
2. V_{DS}=0~400V, I_{SD}≤10A, T_J=25°C;
3. V_{DS}=0~480V
4. Pulse Test: Pulse width≤300us,Duty cycle≤2%;
5. Essentially independent of operating temperature.

8. Typical Characteristics

Figure 1. On-Region Characteristics

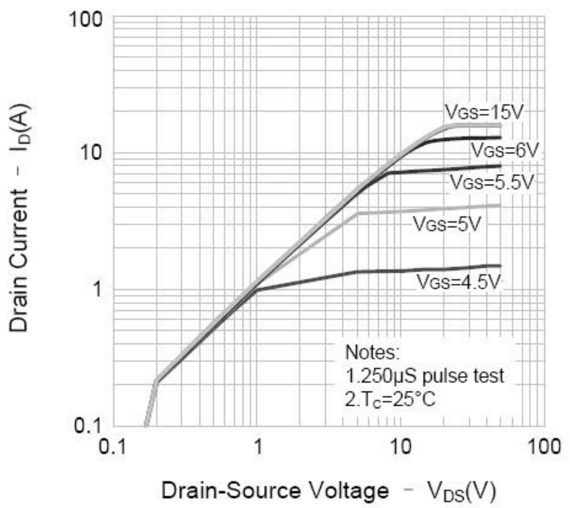


Figure 2. Transfer Characteristics

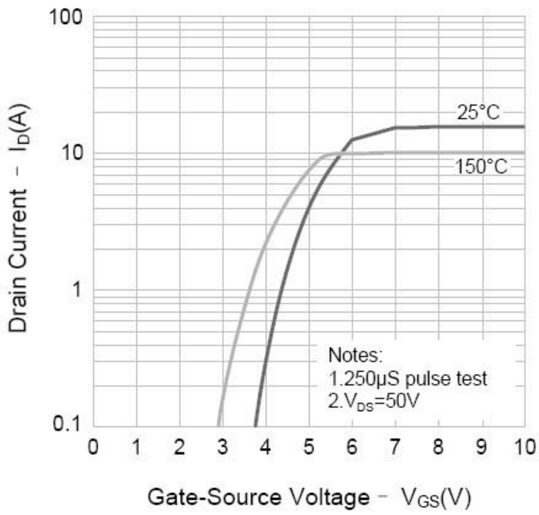


Figure 3. On-Resitance Variation vs. Drain Current and Gate Voltage

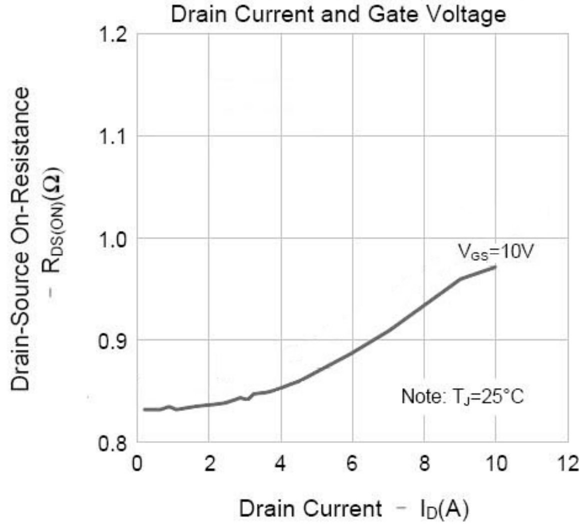


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

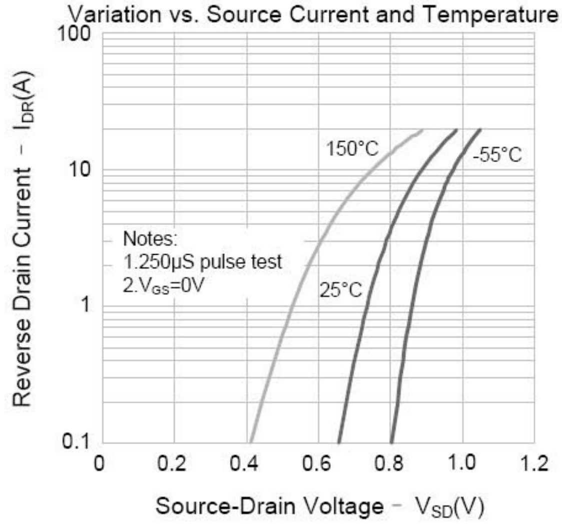


Figure 5. Capacitance Characteristics

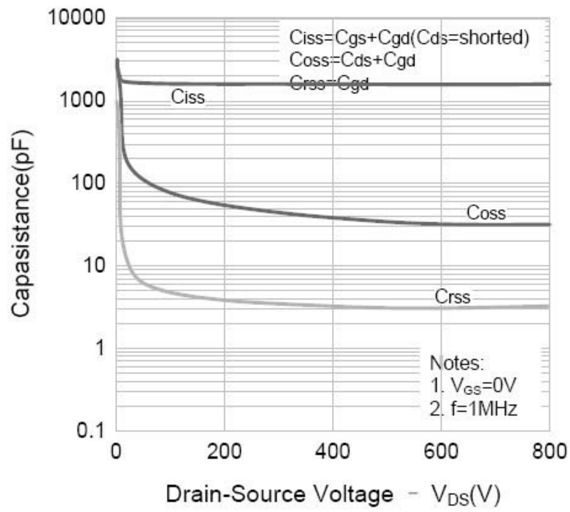


Figure 6. Gate Charge Characteristics

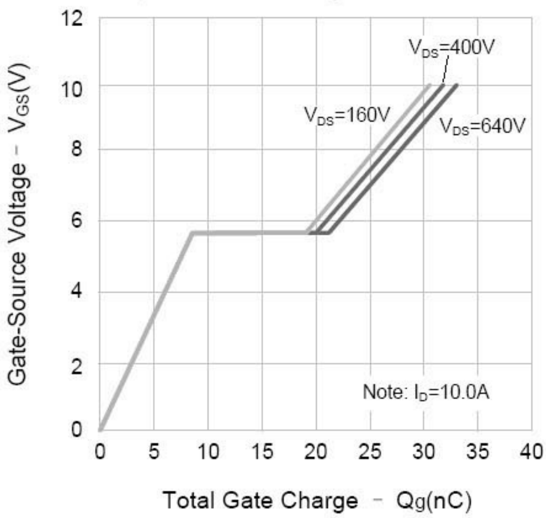


Figure 7. Breakdown Voltage Variation vs. Temperature

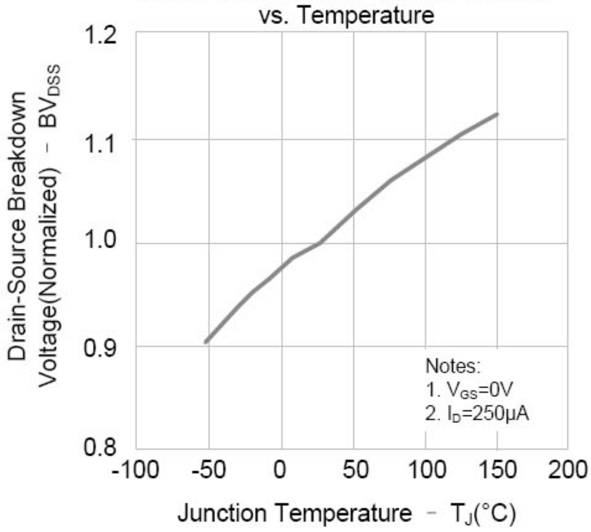


Figure 8. On-resistance Variation vs. Temperature

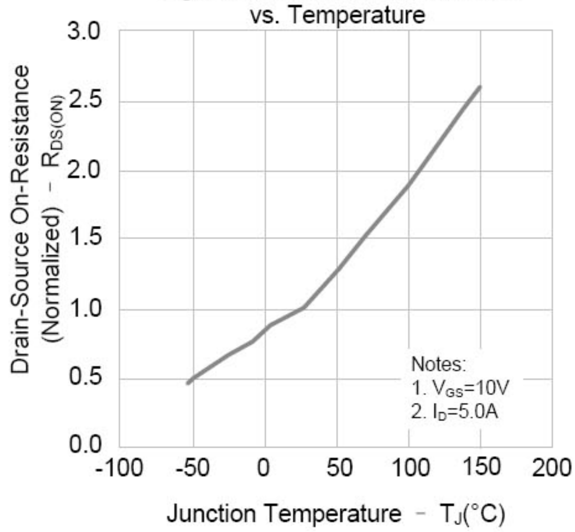


Figure 9-1. Max. Safe Operating Area(SVF10N80F)

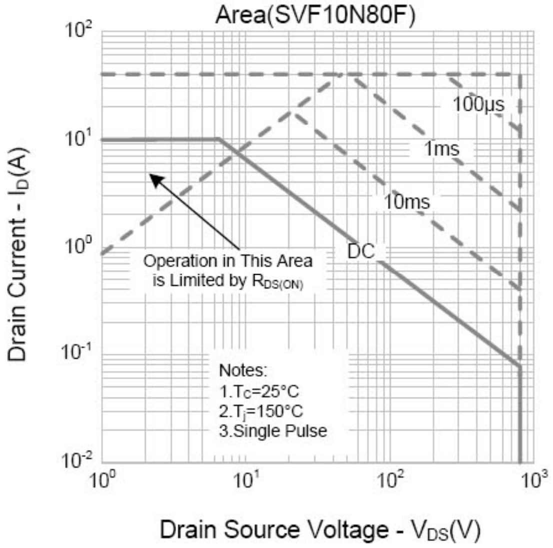


Figure 9-2. Max. Safe Operating Area (SVF10N80K)

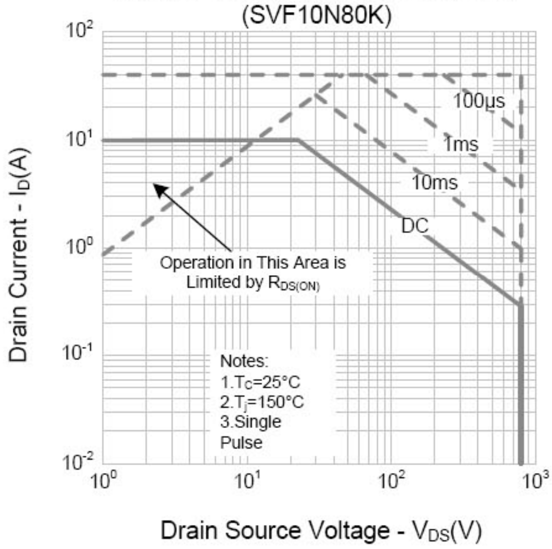
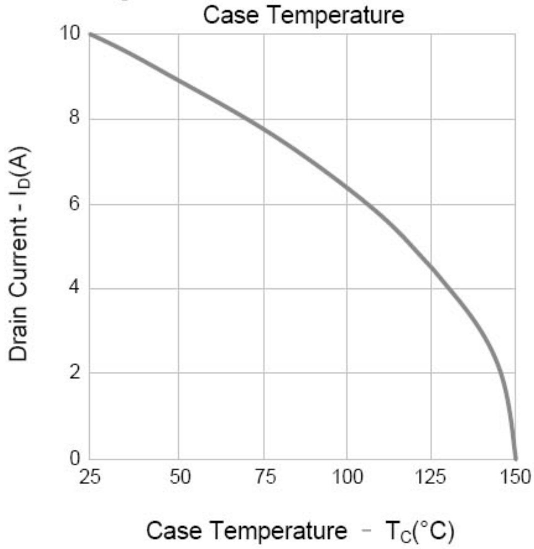
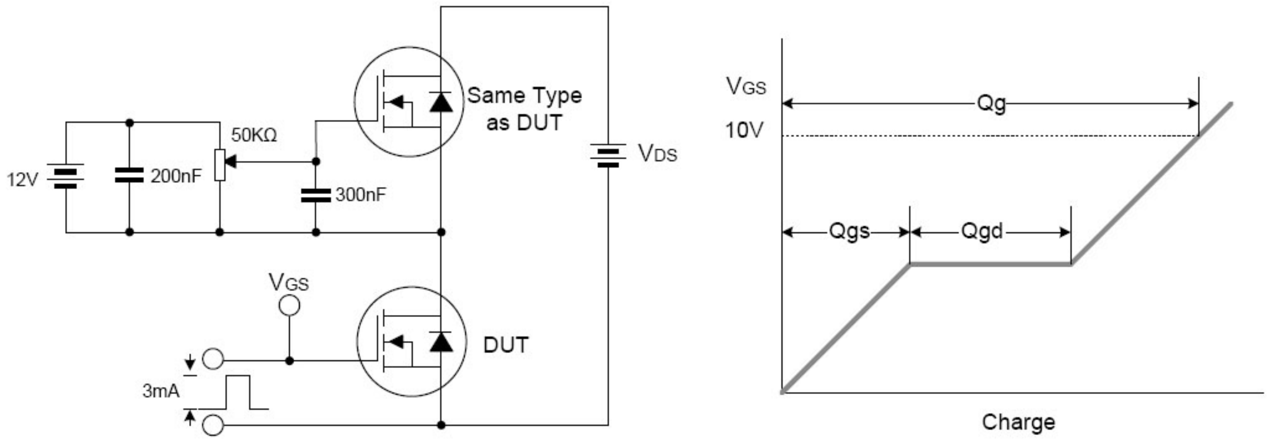


Figure 10. Maximum Drain Current vs. Case Temperature

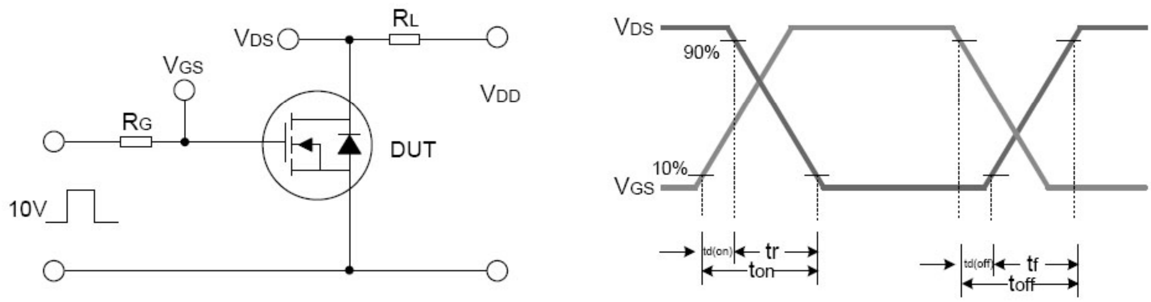


9. Test Circuits and Waveforms

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



Unclamped Inductive Switching Test Circuit & Waveform