

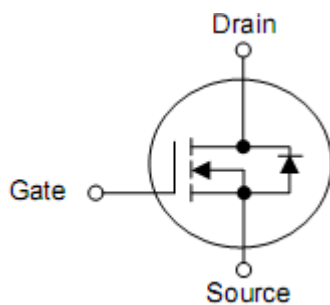
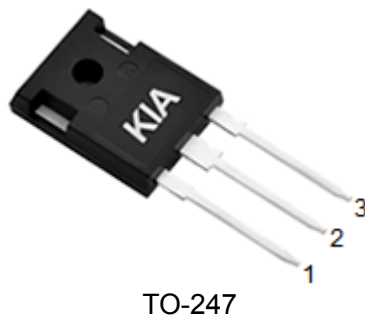
1. Features

- Advanced Planar Process
- $R_{DS(ON)}=650m\Omega(\text{typ.})@V_{GS}=10V$
- Low Gate Charge Minimize Switching Loss
- Rugged Polysilicon Gate Structure

2. Applications

- BLDC Motor Driver
- Electric Welder
- High Efficiency SMPS

3. Symbol



Pin	Function
1	Gate
2	Drain
3	Source

4. Ordering Information

Part Number	Package	Brand
KNM6990A	TO-247	KIA

5. Absolute maximum ratings

$T_C=25^{\circ}\text{C}$ unless otherwise noted

Parameter	Symbol	Rating	Units	
Drain-source voltage	V_{DSS}	900	V	
Gate-to-Source Voltage	V_{GSS}	± 30	V	
Continuous drain current	$T_C=25^{\circ}\text{C}$	I_D	18	A
	$T_C=100^{\circ}\text{C}$	I_D	12	A
Pulsed Drain Current at $V_{GS}=10\text{V}^2)$	I_{DM}	72	A	
Single pulse avalanche energy	E_{AS}	850	mJ	
Peak Diode Recovery dv/dt	dv/dt	5.0	V/ns	
Power dissipation	P_D	625	W	
Derate above 25°C		5.0	W/ $^{\circ}\text{C}$	
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	T_L T_{PAK}	300 260	$^{\circ}\text{C}$	
Operating junction and storage temperature range	T_J, T_{STG}	-55 to 150	$^{\circ}\text{C}$	

Caution: Stresses greater than those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device.

6. Thermal characteristics

Parameter	Symbol	Rating	Unit
Thermal resistance junction-case	$R_{\theta JC}$	0.2	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	55	$^{\circ}\text{C/W}$

7. Electrical characteristics

(T_J=25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	900	-	-	V
Drain-source leakage current	I _{DSS}	V _{DS} =900V, V _{GS} =0V	-	-	1	uA
		V _{DS} =720V, V _{GS} =0V, T _C =125°C	-	-	100	
Gate-source forward leakage	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	-	-	±100	nA
Drain-source on-resistance ³⁾	R _{DS(on)}	V _{GS} =10V, I _D =9A	-	0.65	0.78	Ω
Gate threshold voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250uA	2.5	-	4.5	V
Forward Transconductance	g _{fs}	V _{DS} =20V, I _D =9A	-	10	-	S
Input capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V f=1MHz	-	3790	-	pF
Reverse transfer capacitance	C _{rss}		-	112	-	pF
Output capacitance	C _{oss}		-	255	-	pF
Total gate charge	Q _g	V _{DD} =450V, I _D =18A V _{GS} =0~10V	-	75	-	nC
Gate-source charge	Q _{gs}		-	23.6	-	nC
Gate-drain charge	Q _{gd}		-	22	-	nC
Turn-on delay time	t _{d(on)}	V _{DD} =450V, V _{GS} =10V, R _G =10Ω, I _D =18A	-	37.5	-	ns
Rise time	t _r		-	74.2	-	ns
Turn-off delay time	t _{d(off)}		-	54.6	-	ns
Fall time	t _f		-	58	-	ns
Continuous Source Current ²⁾	I _{SD}	Integral PN-diode in MOSFET	-	-	18	A
Pulsed Source Current ²⁾	I _{SM}		-	-	72	
Diode forward voltage	V _{SD}	I _S =18A, V _{GS} =0V,	-	-	1.4	V
Reverse Recovery Time	t _{rr}	V _{GS} =0V, I _F =18A, dI _F /dt=100A/μs	-	823	-	nS
Reverse Recovery Charge	Q _{rr}		-	8.04	-	nC

Note:

1) T_J=+25 °C to +150 °C

2) Repetitive rating; pulse width limited by maximum junction temperature.

3) Pulse width ≤ 380us; duty cycle ≤ 2%.

8. Typical operating characteristics

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

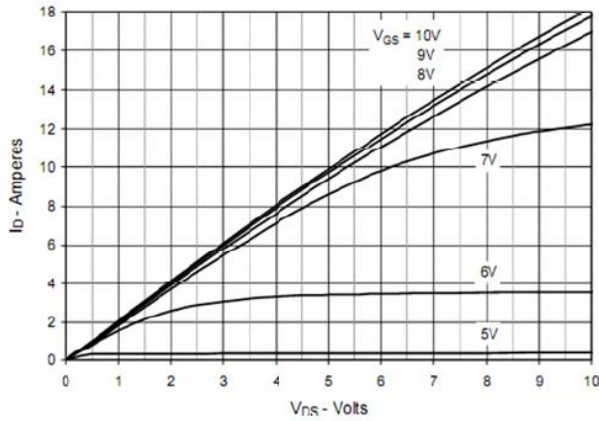


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

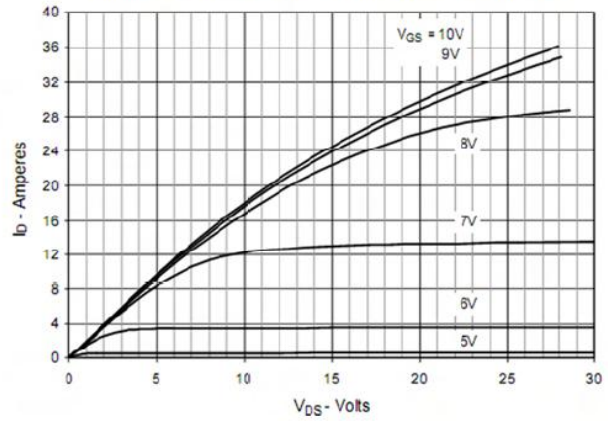


Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

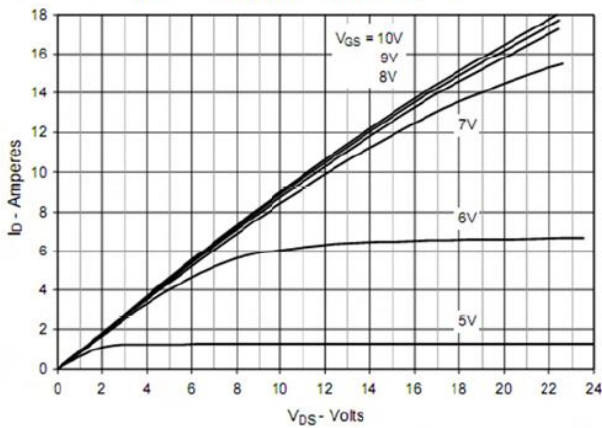


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 9\text{A}$ Value vs. Junction Temperature

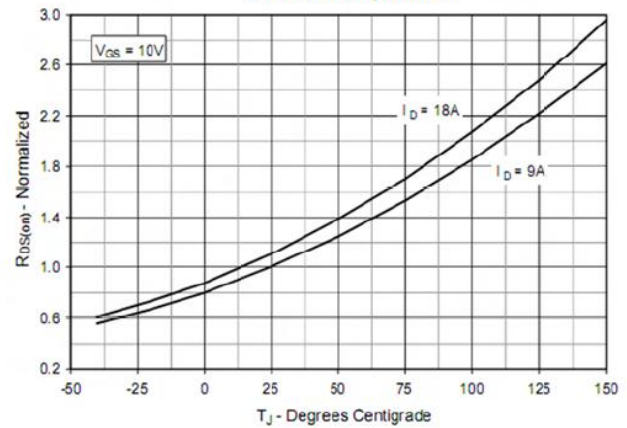


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 9\text{A}$ Value vs. Drain Current

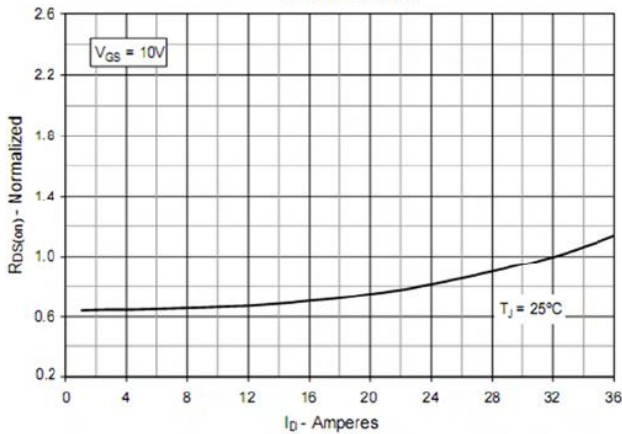


Fig. 6. Maximum Drain Current vs. Case Temperature

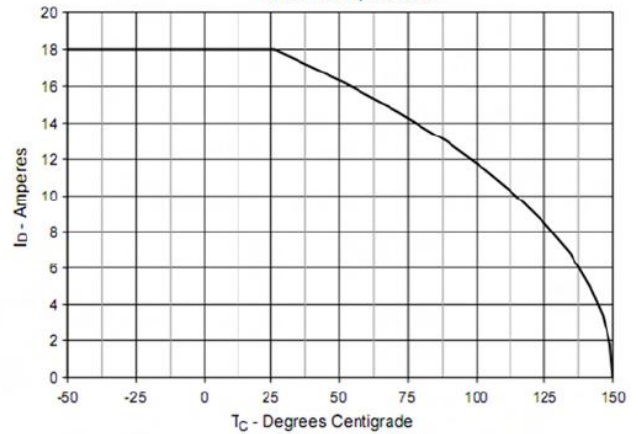


Fig. 7. Input Admittance

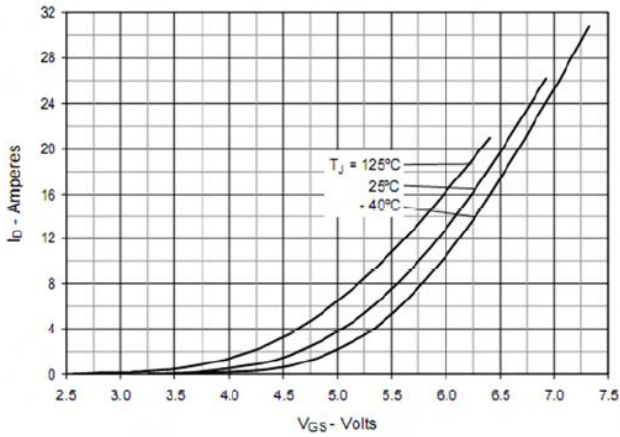


Fig. 8. Transconductance

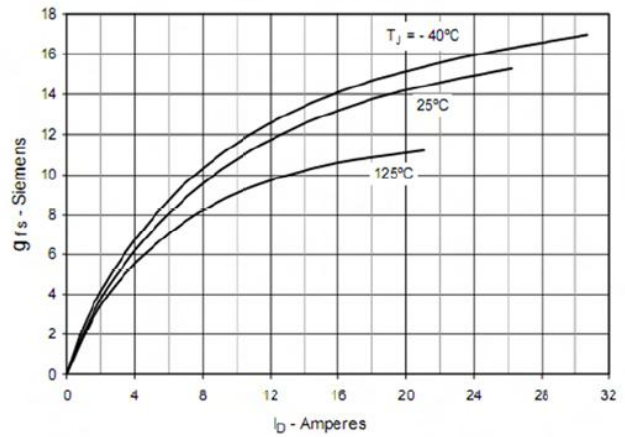


Fig. 9. Forward Voltage Drop of Intrinsic Diode

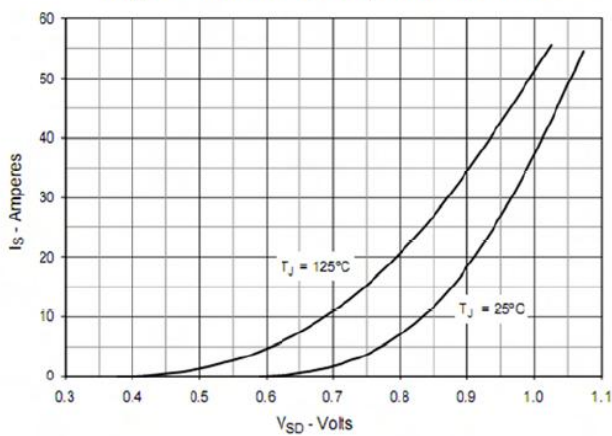


Fig. 10. Gate Charge

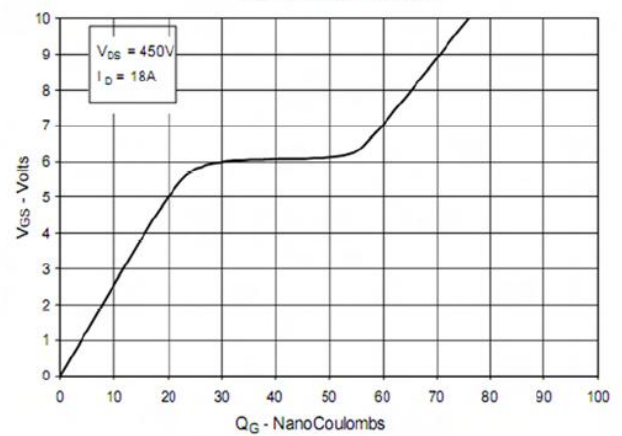


Fig. 11. Capacitance

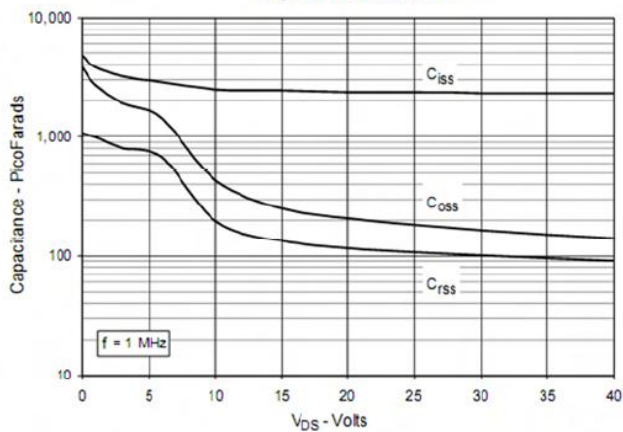
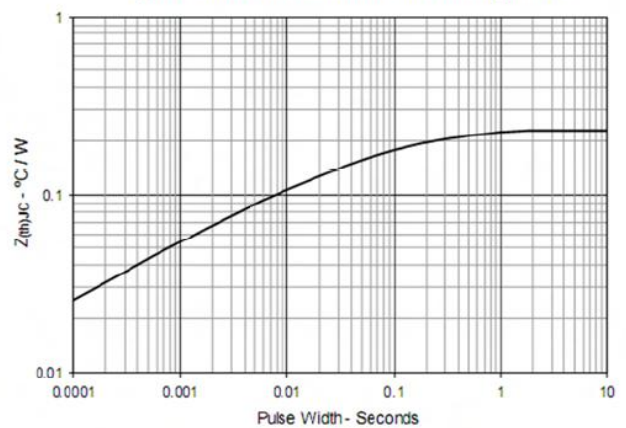


Fig. 12. Maximum Transient Thermal Impedance



9. Test Circuits and Waveforms

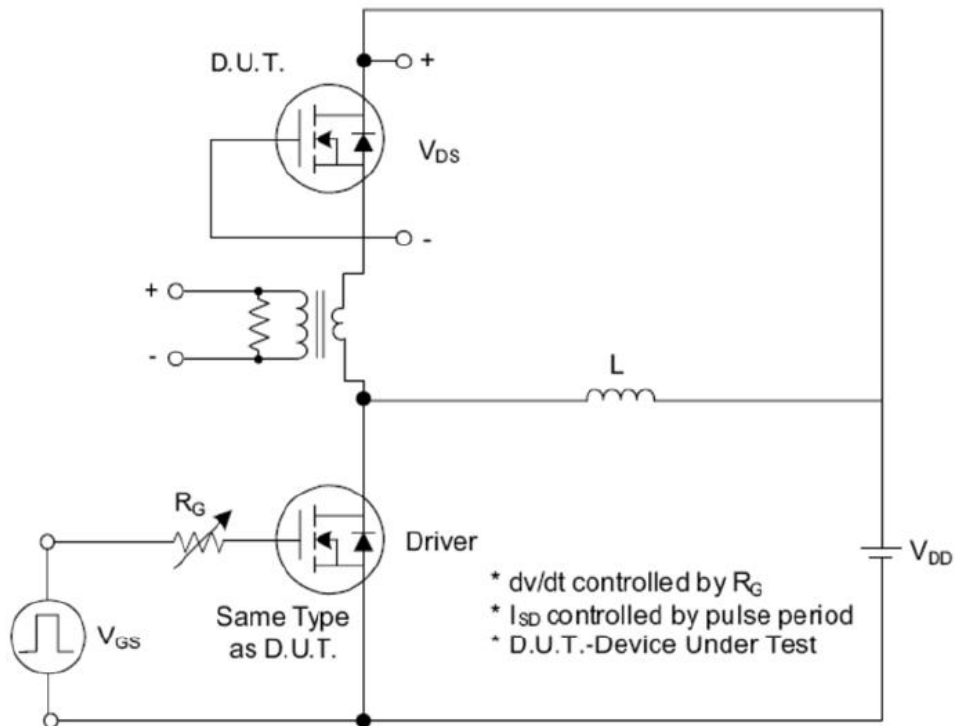


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

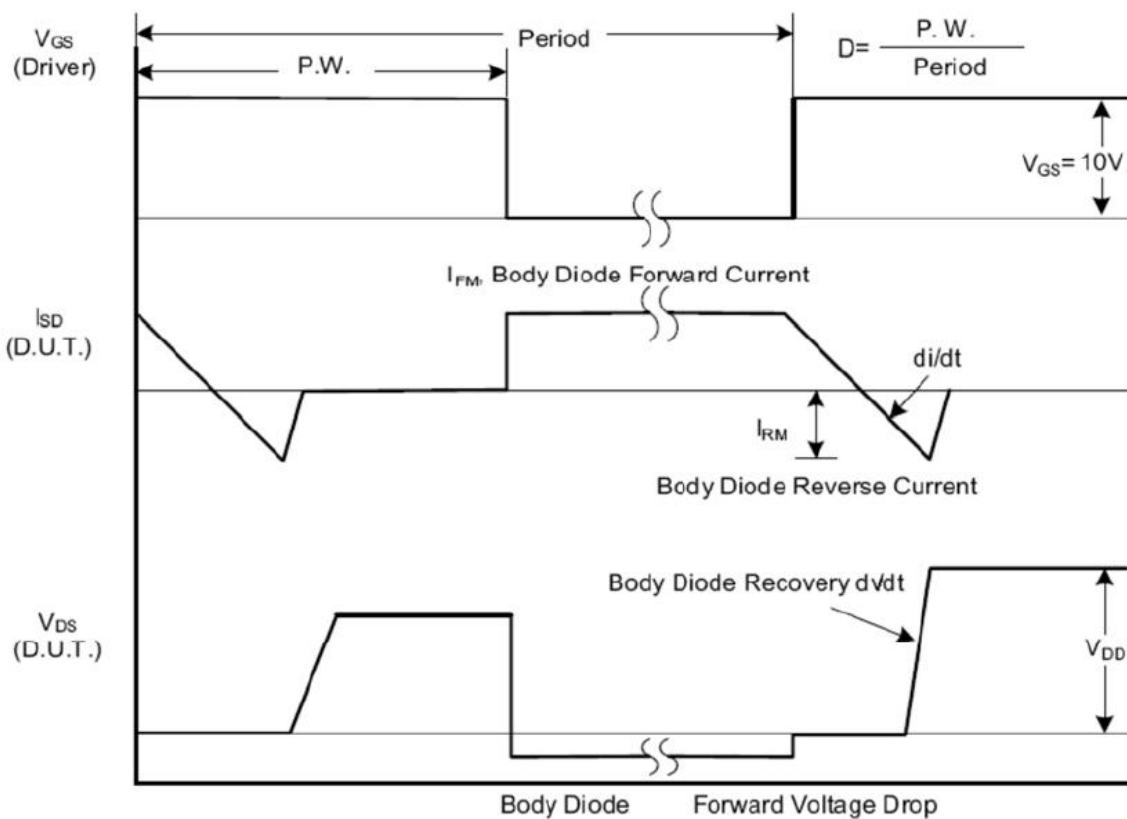


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

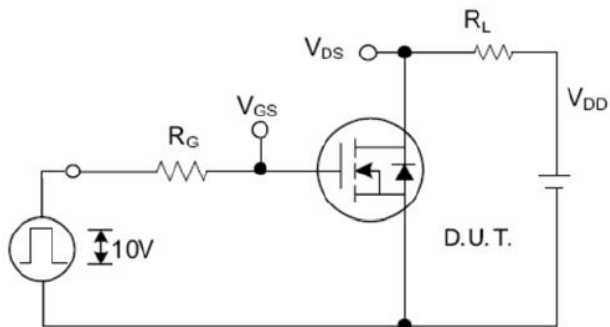


Fig. 2.1 Switching Test Circuit

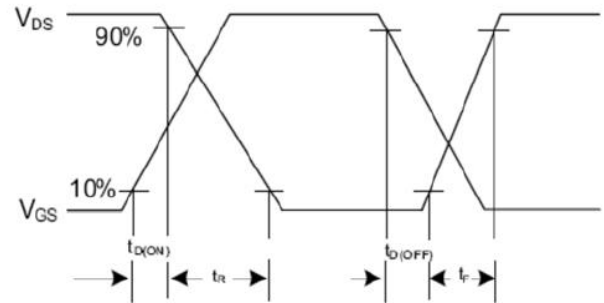


Fig. 2.2 Switching Waveforms

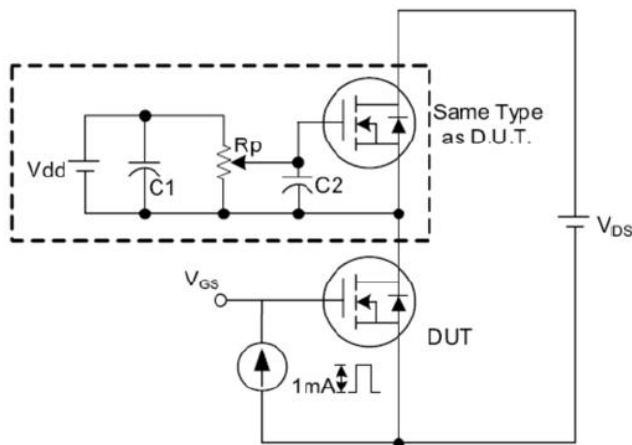


Fig. 3.1 Gate Charge Test Circuit

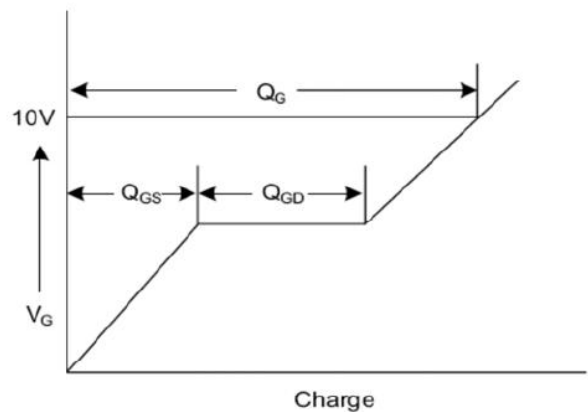


Fig. 3.2 Gate Charge Waveform

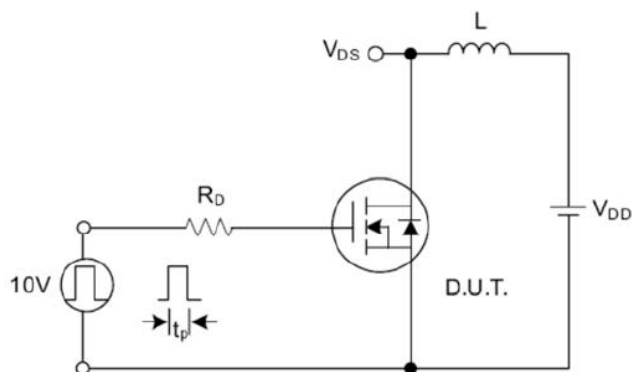


Fig. 4.1 Unclamped Inductive Switching Test Circuit

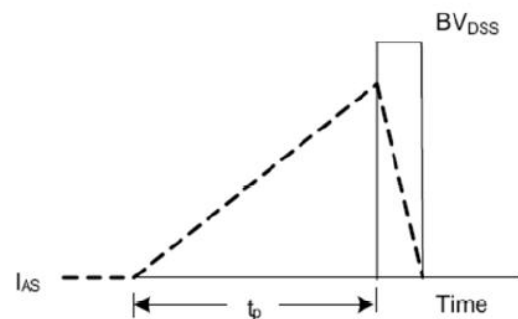


Fig. 4.2 Unclamped Inductive Switching Waveforms